CLAIMS

We claim:

1. A method for testing first and second sets of electronic devices on a microchip, the first set of devices receiving input data and then sending output data to a first MISR, the second set of devices receiving input data and then sending output data to a second MISR, the method comprising:

    determining a first seed signature value associated with the first MISR that induces the first MISR to have a first final signature value comprising a plurality of identical binary values when the first set of devices send valid output data to the first MISR when receiving a first predetermined sequence of input data;

    determining a second seed signature value associated with the second MISR that induces the second MISR to have a second final signature value comprising a plurality of identical binary values when the second set of devices send valid output data to the second MISR when receiving a second predetermined sequence of input data;

    initializing first and second states of the first MISR and the second MISR, respectively, to the first and second signature values, respectively;

    inputting the first and second predetermined sequences of input data to the first and second set of devices, respectively, and generating first and second final signatures values from output data received from the first and second set of devices, respectively; and,

    indicating that the first and second set of devices have failed testing when at least one of the plurality of binary values in the first and second final signature values are not identical.

2. The method of claim 1 further comprising indicating that first and second sets of devices have passed testing when each of the plurality of binary values in the first and second final signature values have an identical binary value.

3.   The method of claim 2 wherein the each of the plurality of binary values in the first and second final signature values have a binary value of 1 when the first and second set of devices passed testing.

4.   The method of claim 2 wherein the each of the plurality of binary values in the first and second final signature values have a binary value of 0 when the first and second set of devices passed testing.

5.   The method of claim 1 wherein each of the first and second set of electronic devices include at least one of combinatorial logic devices, sequential logic devices, memory arrays.

6.   The method of claim 1 wherein each of the first and second set of electronic devices comprise memory arrays.

7.   The method of claim 1 wherein the step of determining a first seed signature value, comprises:

determining an expected signature value indicative of the first set of devices passing testing;

calculating a second value corresponding to a Boolean complement of the expected signature value; and,

selecting the first seed signature value from a sequence of output values generated by a LFSR receiving no data, the selection being based on a position of the second value in the sequence of output values.

8.   The method of claim 1 wherein the step of determining a first seed signature value, comprises:

determining an expected signature value indicative of the first set of devices passing testing; and,

selecting the first initial output signature value from a sequence of output values generated by a LFSR receiving no data, the selection being based on a position of the expected signature value in the sequence of output values.

9.   The method of claim 1 wherein the first predetermined sequence of input data comprises a sequence of binary numbers.

10.   A system for testing first and second sets of electronic devices on a microchip, comprising:

a test computer operatively coupled to a first LFSR, a second LFSR, a first MISR, and a second MISR, the test computer configured to determine a first seed signature value associated with the first MISR that induces the first MISR to have a first final signature value comprising a plurality of identical binary values when the first set of devices send valid output data to the first MISR when receiving a first predetermined sequence of input data, the test computer further configured to determine a second seed signature value associated with the second MISR that induces the second MISR to have a second final signature value comprising a plurality of identical binary values when the second set of devices send valid output data to the second MISR when receiving a second predetermined sequence of input data, the test computer further configured to initialize first and second states of the first and second MISRs, respectively, to the first and second seed signature values, respectively;

a first LFSR configured to transmit the first predetermined sequence of test data to the first set of devices;

a second LFSR configured to transmit the second predetermined sequence of test data to the second set of devices;

the first and second MISRs configured to generate first and second final signature values from the output data received from the first and second set of devices, respectively; and,

a circuit configured to indicate the first and second set of devices have failed testing when at least one of the plurality of binary values in the first and second final output signature values are not identical.

11. The system of claim 10 wherein the circuit further indicates the first and second sets of devices have passed testing when each of the plurality of binary values in the first and second final signature values have an identical binary value.

12. The system of claim 10 wherein each of the plurality of binary values in the first and second final signature values have a binary value of 0 when the first and second set of devices passed testing.

13. The system of claim 10 wherein each of the first and second set of electronic devices include at least one of combinatorial logic devices, sequential logic devices, memory arrays.

14. The system of claim 10 wherein each of the first and second set of electronic devices comprise memory arrays.

15. The system of claim 10 wherein the circuit comprises:

a first OR logic gate receiving each binary value associated with the first final signature value and generating a first binary value;

a second OR logic gate receiving each binary value associated with the second final signature value and generating a second binary value; and,

a third OR logic gate receiving the first and second binary values and generating a third binary value indicative of whether the first and second sets of devices passed the testing.

16.   The system of claim 10 wherein the test computer is further configured to determine an expected signature value indicative of the first set of devices passing testing, the test computer further configured to calculate a second value corresponding to a Boolean complement of the expected signature value, and the test computer further configured to select the first seed signature value from a sequence of output values generated by a LFSR receiving no data, the selection being based on a position of the second value in the sequence of output values.

17.   The system of claim 10 wherein the test computer is further configured to determine an expected signature value indicative of the first set of devices passing testing, the test computer further configured to select the first seed signature value from a sequence of output values generated by a LFSR receiving no data, the selection being based on a position of the expected signature value in the sequence of output values.

18.   The system of claim 10 wherein the first predetermined sequence of input data comprises a sequence of binary numbers.

19.   The system of claim 10 wherein the circuit comprises:

a first AND logic gate receiving each binary value associated with the first final signature value and generating a first binary value;

a second AND logic gate receiving each binary value associated with the second final signature value and generating a second binary value; and,

a third AND logic gate receiving the first and second binary values and generating a third binary value indicative of whether the first and second sets of devices passed the testing.

20.   A system for testing first and second sets of electronic devices on a microchip, comprising:

a first MISR having a first seed signature value to obtain a first final signature value comprising a plurality of identical binary values when the first set of devices send valid output data to the first MISR;

a second MISR being having a second seed signature value to obtain a second final signature value comprising a plurality of identical binary values when the second set of devices send valid output data to the second MISR;

at least one apparatus configured to transmit the first predetermined sequence of test data to the first set of devices and a second predetermined sequence of test data to the second set of devices;

the first and second MISRs configured to generate first and second final signature values from the output data received from the first and second set of devices, respectively; and,

a circuit configured to indicate the first and second set of devices have failed testing when at least one of the plurality of binary values in the first and second final output signature values are not identical.